

## **CLAIMS**

## WHAT IS CLAIMED:

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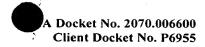
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1	1.	A built-in sen-test controller, comprising.	
2	a built-in self-test engine capable of executing a built-in self-test and generating ar		
3		indication of whether the executed built-in self-test is completed; and	
4	a buil	t-in self-test signature including the indication.	
1	2.	The built-in self-test controller of claim 1, wherein the built-in self-test engine	
2	is a logic built-in self-test engine and the built-in self-test signature is a logic built-in self-test		
3	signature.		
	3.	The built-in self-test controller of claim 2, wherein the logic built-in self-test	
2 3 3 4	engine comprises:		
	a logic built-in self-test state machine; and		
	a pattern generator.		
1=	4.	The built-in self-test controller of claim 3, wherein the logic built-in self-test	
!! 2.£	state machine further comprises:		
3	a reset state entered upon receipt of an external reset signal;		
41	an initiate state entered from the reset state upon receipt of a logic built-in self-test run		
3 &		signal;	
6	a sca	n state entered from the initiate state upon the initialization of components and	
7		signals in the logic built-in self-test domain in the initiate state;	
8	a step state entered into from the scan state and from which the scan state is entered		
9		unless the content of the pattern generator equals a predetermined vector	
10		count; and	
l 1	a done state entered into when the content of the pattern generator equals the		
12		predetermined vector count.	

5. The built-in self-test controller of claim 1, wherein the logic built-in self-test signature comprises the content of a multiple input signature register.

in self-test engines comprises:

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3	a reset state entered upon receipt of an external reset signal;	
4 .	an initiate state entered from the reset state upon receipt of at least one of a memory	
5	built-in self-test run signal and a memory built-in self-test select signal;	
6	a flush state entered from the initiate state upon the initialization of components and	
7	signals in the memory built-in self-test domain in the initiate state;	
8	a test state entered into from the flush state; and	
9	a done state entered into upon completing the test of each of a plurality of memory	
10	components in the memory built-in self-test.	
1	13. A built-in self-test controller, comprising:	
2	means for executing a built-in self-test and generating an indication of whether the	
3	executed built-in self-test is completed; and	
4,5	means for storing the results of the executed built-in self-test, including the indication.	
ı J	14. The built-in self-test controller of claim 13, wherein the executing means is a	
	logic built-in self-test engine and the storing means is a logic built-in self-test register.	
i).	15. The built-in self-test controller of claim 13, wherein the storing means	
2 	comprises the content of a multiple input signature register.	
1	16. The built-in self-test controller of claim 13, wherein the executing means is a	
2	memory built-in self-test engine and the storing means is a memory built-in self-test signature	
3=4	register.	
1	17. An integrated circuit device, comprising:	
2	a plurality of memory components;	
3	a logic core;	
4	a testing interface; and	
5	a built-in self-test controller, including:	
6	a built-in self-test engine capable of executing a built-in self-test on one of the	
7	memory components and the logic core and storing the results thereof,	
8	wherein the results include an indication of whether an executed built-	
9	in self-test is completed; and	
10	a register capable of storing the results of an executed built-in self-test,	
11	including the indication.	

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- 18. The integrated circuit device of claim 17, wherein the built-in self-test engine is a logic built-in self-test engine and the register is a multiple input signature register.
- 19. The integrated circuit device of claim 17, wherein the built-in self-test engine is a memory built-in self-test engine and the register is a memory built-in self-test signature register.
- 20. The integrated circuit device of claim 17, wherein the memory components include a static random access memory device.
- 21. The integrated circuit device of claim 17, wherein testing interface comprises a Joint Test Action Group tap controller.
  - 22. A method for performing a built-in self-test, the method comprising: performing a built-in self-test, including generating a indication of whether the built-in self-test is completed; and storing the indication.
- 23. The method of claim 22, wherein performing the built-in self-test includes performing a logic built-in self-test and storing the indication includes setting a bit in a multiple input signature register.
- 24. The method of claim 23, wherein performing the logic built-in self-test includes:

resetting a logic built-in self-test engine;

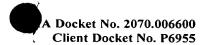
initiating a plurality of components and signals in a built-in self-test controller upon receipt of a logic built-in self-test run signal;

scanning a scan chain upon the initialization of the components and the signals;

stepping to a new scan chain; and

repeating the previous scanning and stepping until the content of a pattern generator in a logic built-in self-test engine of the built-in self-test controller equals a predetermined vector count.

25. The method of claim 23, further comprising at least one of: setting a bit in the multiple input signature register indicating an error condition arose; and



setting a bit in the multiple input signature register indicating whether the stored 4 results are from a previous logic built-in self-test run. 5 26. The method of claim 22, wherein performing the built-in self-test includes performing a memory built-in self-test and storing the indication includes setting a bit in a 2 memory built-in self-test signature register. 3 27. The method of claim 26, wherein performing the memory built-in self-test 1 includes: 2 resetting a memory built-in self-test engine; initiating a plurality of components and signals in a built-in self-test controller upon receipt of at least one of a memory built-in self-test run signal and a memory 5 built-in self-test select signal; 7 8 9 4 4 4 4 5 flushing the contents of a plurality of memory components to a known state after initialization of the components and the signals; and testing the flushed memory components. 28. The method of claim 26, wherein performing the memory built-in self-test further includes at least one of: storing the results of the memory built-in self-test in the memory built-in self-test signature register; and storing the results of at least one paranoid check in the memory built-in self-test signature register. 29. A method for testing an integrated circuit device, the method comprising: interfacing the integrated circuit device with a tester; 2 performing a built-in self-test, including generating a indication of whether the built-3 in self-test is completed; storing the indication; and 5 reading the indication. 30. The method of claim 29, wherein performing the built-in self-test includes 1 performing a logic built-in self-test and storing the indication includes setting a bit in a 2

multiple input signature register.

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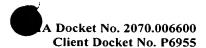
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- 31. The method of claim 29, wherein performing the built-in self-test includes performing a memory built-in self-test and storing the indication includes setting a bit in a memory built-in self-test signature register.
- 32. The method of claim 29, wherein interfacing the integrated circuit device with the tester includes employing Joint Test Action Group protocols.